Gate Power Dissipation

Every digital gate will require some amount of **power**. It must **dissipate** this power in the form of heat. We consider **two** types of power:

Static P_D - Power dissipated when gate **is not** changing state.

Dynamic P_D - Power dissipated when gate **is** changing states.

Typically we find that:

$$\text{Dynamic } P_D \geq \text{Static } P_D$$

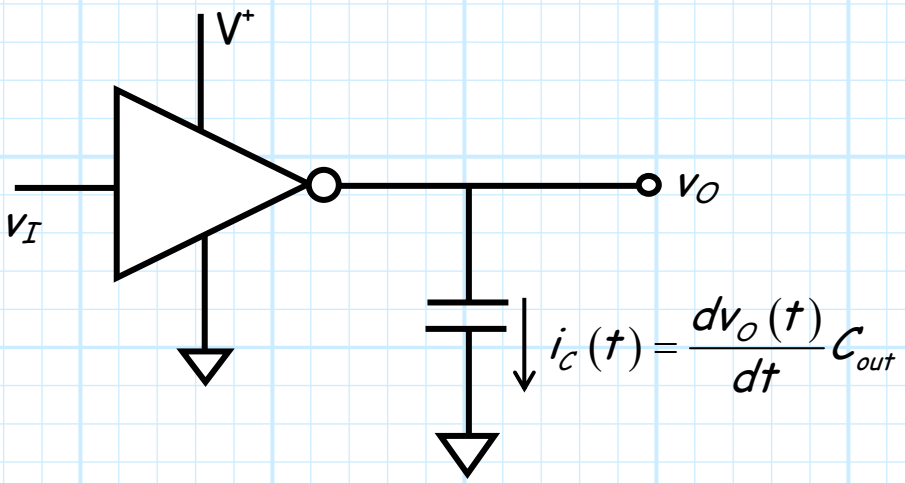
In fact, for CMOS logic gates (e.g., a CMOS digital inverter), we will find that the **static** P_D is nearly **zero**!

However, we will find that it **always** takes some power to **change** the output state of a digital logic gate.

Q: *Why is that??*

A: **Capacitance**! When we change the **voltage** at the output, we must charge or discharge the **capacitance** associated with the output. This requires **current**!

Although engineers work very hard to **minimize** the output capacitance of digital circuits, we **cannot** fully eliminate it.



Note that the **displacement current** $i_C(t)$ flowing "through" this capacitor is proportional to the **time derivative** of the output voltage.

* Thus, if the output state is **static** (i.e., it is not changing), this derivative is **zero**, as is the current.

* However, if the output is **dynamic** (i.e. it is changing with time), the derivative is **non-zero**, and thus displacement current **flows** in the capacitor.

* Note that the **faster** we change the output, the **more** displacement current is produced, meaning **more power** is required!

* Thus, we come to the (correct) conclusion that **dynamic** power dissipation is **dependent** on the speed (e.g., clock frequency) of the digital logic—the "**faster**" the logic, the **higher** the dynamic power dissipation!

* As a result, dynamic P_D is typically **specified** as a function of **frequency**.